IN THE CLAIMS

Please amend the claims as follows. Presented below is a complete listing of claims in the revised format showing markings as set forth by the U.S. Patent and Trademark Office on January 31, 2003:

Claims 1-3 (Canceled)

4. (Withdrawn) A method of initializing a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

selecting one of a plurality of clocks before configuring the CSL;

configuring the CSL; and

selecting one of the plurality of clocks after configuring the CSL.

5. (Withdrawn) A method of initializing a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

checking for one of a serial and a parallel output device external to the CSoC and coupled to a memory interface unit (MIU) in the CSoC;

setting the MIU to an appropriate mode based on the output device;

searching for a header in the output device;

switching to another mode if the header is not found; and

configuring the CSL if the header is found.

E

6. (Withdrawn) The method of Claim 5, wherein if the header is not found in the other mode, then further including:

checking whether the output device is accessible;

powering down the CSoC if the output device is accessible; and

repeating the steps in Claim 5 if the output device is not accessible.

7. (Withdrawn) A programmable interconnect structure providing a signal to a logic block, the interconnect structure comprising:

a plurality of interconnect lines divided into sets of interconnect lines;

a plurality of first-tier multiplexers, each first-tier multiplexer having input terminals coupled to a set of interconnect lines and having an output terminal;

a plurality of second-tier multiplexers, each second-tier having a first input terminal coupled to one output terminal of the first-tier multiplexers and a second input terminal coupled to a constant voltage source,

wherein the plurality of second-tier multiplexers selectively provide output signals from the first terminals or the second terminals to the logic block.

8. (Withdrawn) A method of providing signals to a logic block, the method comprising:

selectively providing one of a plurality of interconnect signals and a constant logic signal to the logic block,

wherein during a configuration mode, the constant logic signal is provided to the logic block, and

E

wherein during a user mode, the plurality of interconnect signals are provided to the logic block.

9. (Withdrawn) An input multiplexer to a logic block, the input multiplexer comprising:

a first multiplexer receiving a first plurality of input signals and a constant signal;

a second multiplexer receiving a second plurality of input signals and a mode signal;

a third multiplexer receiving output signals from the first and second multiplexers and providing an output signal on a logic block input line; and

a first transistor coupled to an internal logic block line, the first transistor controlled by the mode signal.

10. (Withdrawn) A method of providing signals on an internal logic block line of a logic block, the method comprising:

providing a plurality of input signals to a plurality of selectors, wherein each selector further receives one of a constant logic value and a mode signal;

selectively providing one of the plurality of input signals, the constant logic value, and the mode signal on the internal logic block line, wherein the mode signal indicates whether the logic block is in a configuration mode or a user mode.

11. (Withdrawn) The method of Claim 10, wherein during configuration, the plurality of input signals, the constant logic value, and the mode signal have the same value.

E

12. (Withdrawn) The method of Claim 10, wherein during the user mode, the constant logic value and the mode signal have different values.

13. (Withdrawn) The method of Claim 10, further including using the mode signal to transfer the constant logic value to the internal logic block line.

14. (Currently Amended) The method of claim ~~13~~ 20 further comprising:

mapping the memory cell in the CSL into an addressable memory space of the system bus.

15. (Previously Presented) The method of claim ~~14~~ wherein reading a memory cell in the CSL using the system bus is performed by a second device selected from the group consisting of the CPU, the direct memory access (DMA) controller, and the external control device.

16. (Previously Presented) The method of claim ~~15~~ further comprising:

mapping a random access memory (RAM) cell in the CSoC into the addressable memory space of the system bus.

17. (Previously Presented) The method of claim ~~16~~ further comprising:

reading the RAM cell using the system bus.

18. (Previously Presented) The method of claim ~~17~~ wherein reading the RAM cell using the system bus is performed by a third device selected from the group consisting of the CPU, the direct memory access (DMA) controller, and the external control device.

19. (Canceled)

20. (Currently Amended) ~~The~~ A method of ~~claim 19 further~~ using a multi-master system bus on a configurable system on a chip (CSoC), the CSoC including configurable system logic (CSL), the method comprising:

controlling the multi-master system bus for configuration using a first device, the first device comprising a selectable one of an on-chip central processing unit (CPU), a direct memory access (DMA) controller, and an external control device;

configuring a memory cell in the CSL using the multi-master system bus;

reading the memory cell in the CSL using the multi-master system bus; and

selecting a signal with a multiplexer in the CSoC to determine if the system bus is used for configuration or general interconnect.

21. (Currently Amended) A method of configuring a configurable system on a chip (CsoC) comprising:

initiating configuration of the CsoC using an on-chip central processing unit (CPU);

passing control of a multi-master system bus to a first device for configuring on-chip configurable system logic (CSL);

configuring a memory cell in the CSL using the first device;

selecting a signal with a multiplexer in the CSoC to determine if the system bus is used for configuration or general interconnect.

22. (Previously Presented) The method of claim 21, wherein the first device is selected from a group consisting of the CPU, a direct memory access (DMA) controller, and an external control device.

23. (Previously Presented) The method of claim 21 further comprising:

reading a memory cell in the CSL using a second device selected from a group consisting of the CPU, a direct memory access (DMA) controller, and an external control device.

24. (Previously Presented) The method of claim 21 further comprising:

mapping the memory cell in the CSL into an addressable memory space of the system bus.

25. (Previously Presented) The method of claim 24 further comprising:

mapping a random access memory (RAM) cell in the CSoC into the addressable memory space of the system bus.

26. (Previously Presented) The method of claim 25 further comprising:

reading the RAM cell using the system bus.

27. (Previously Presented) The method of claim 26, wherein reading the RAM cell using the system bus is performed by a third device selected from the group consisting of the CPU, a direct memory access (DMA) controller, and an external control device.

28. (Previously Presented) The method of claim 21 wherein the system bus is used for configuration and general interconnect of the CSoC.

29. (Previously Presented) The method of claim 28 further comprising:

selecting a signal in the CSoC to indicate that the system bus is being used for configuration rather than general interconnect of the CSoC.

30. (Currently Amended) A method comprising:

initiating configuration of a configurable system on chip (CsoC) using an on-chip central processing unit (CPU);

configuring a memory cell in the CSL using a first device of a group of devices, the group of devices comprising the CPU, a direct memory access (DMA) controller, and an external control device;

reading a memory cell in the CSL using a second device selected from the group of devices; and

selecting a signal with a multiplexer in the CSoC to determine if ~~the~~ a system bus is used for configuration or general interconnect of the CSoC.

31. (Previously Presented) The method of claim 30, wherein the first device and the second device are the same device.

32. (Previously Presented) The method of claim 30, wherein control of ~~a~~ the system bus on the CSoC is by the on-chip CPU, the first device, or the second device based on which device is performing operations on the CSL.